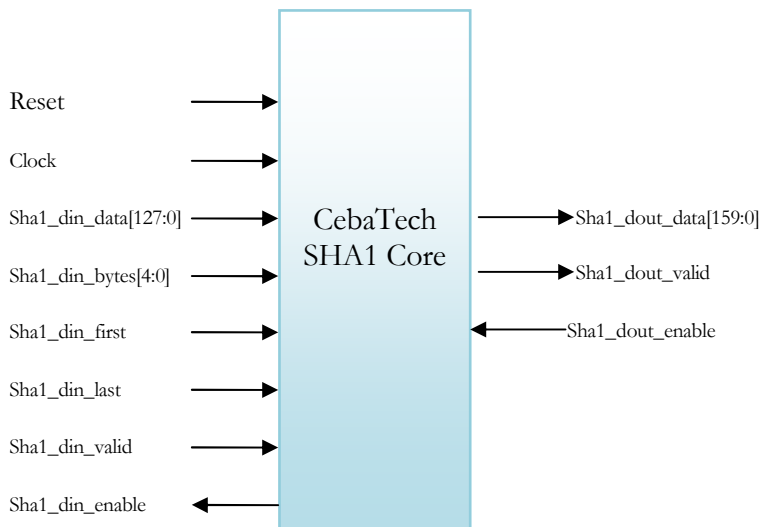


### Overview

CebaTech's SHA-1 cores are a direct hardware embodiment of NIST's original software implementation as defined in FIPS PUB 180-1, enabling a state of the art FPGA or ASIC solution for cryptographic hash function with 160-bit hash value. CebaTech's hardware implementation of SHA-1 is in the form of standalone soft cores that perform the cryptographic hash function. CebaTech's SHA-1 cores precisely follow the data formats defined by the software algorithm.

CebaTech's SHA-1 cores are designed to reduce the processing overhead of high-speed data hashing.



### Deliverables

- Synthesizable Verilog™ RTL Source.
- Comprehensive User's Guide.
- Simulation Environment and Scripts.
- Test Files.

### CebaTech's SHA-1 Features

- Self-contained, standalone soft core that performs the hash function.
- Fully compliant with FIPS PUB 180.
- Fully conformant with NIST's software algorithm.
- Suitable for FPGA and ASIC targets.
- Fully synchronous design.
- Low number of cycles.
- Auto padding.



## Resource Requirements

Cebatech's SHA-1 IP core targets both ASIC or FPGA applications. Cebatech's unique ESL flow allows timing, area and performance optimizations based on customer's requirements. For information related to your specific application needs, please contact us at [sales@cebatech.com](mailto:sales@cebatech.com).

### **About Cebatech**

**Headquartered in Eatontown, NJ, Cebatech, Inc. is a privately held, venture-backed company focused on developing ESL tools and intellectual property modules that accelerate the development and realization of complex software algorithms in silicon. Information about the company and its products may be found at [www.cebatech.com](http://www.cebatech.com)**

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