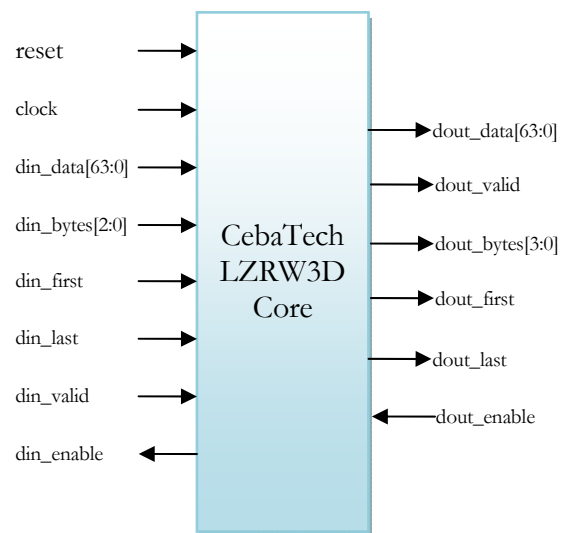
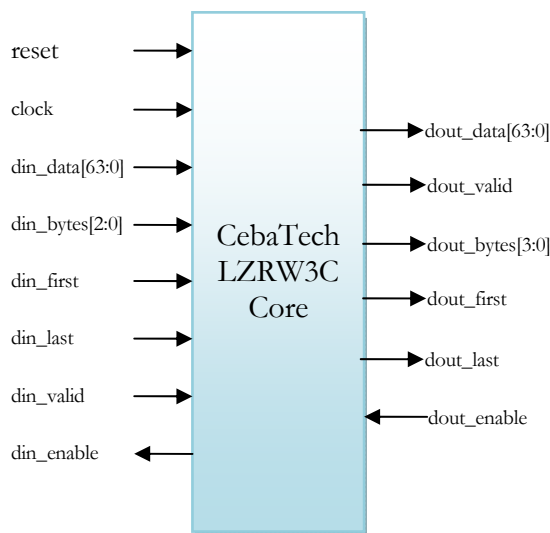


Overview

CebaTech's LZRW3 cores are a direct hardware embodiment of Ross Williams' original software implementation, enabling a state of the art FPGA or ASIC solution for wire-speed lossless data compression and decompression. CebaTech's hardware implementation of LZRW3 is in the form of standalone soft cores that perform the compress and expand functions.

CebaTech's LZRW3 cores are designed to reduce the processing overhead of high-speed data compression and improve the performance of data and storage networking appliances and systems.



CebaTech's LZRW3 Features

- Self-contained, standalone soft core suitable for ASIC and FPGA targets.
- Fully synchronous design.
- Fully conformant with Ross Williams' software algorithm.
- Capable of data throughputs in excess of 2Gbps.
- Compression ratios of 2:1 and greater.
- Stream interface or PCI-core interface.

Deliverables

- Synthesizable Verilog™ RTL Source.
- Comprehensive User's Guide.
- Simulation Environment and Scripts.
- Test Files.

LZRW3 Compression/Decompression

The LZRW3 algorithm was developed by Ross Williams in the 1990's and is implemented using a variation of LZ (Lempel-Ziv). The algorithm offers high throughput with good compression by finding duplicated strings in the input data. The second occurrence of a string is replaced by a length and an index. The index is used to address a hash table containing an offset into the input data window. The hash table is not transmitted with the compressed data. An identical table is generated on the fly by the de-compressor.

LZRW3 Configuration and Performance

Multiple configuration options for CebaTech's LZRW3 core allow the core to be matched with the user application. Configuration time options determine how the core is built, and impact performance in terms of compression, throughput and area.

History Window Size

Users can select their history window size to match the application, or they can trade off area in exchange for performance. The history table represents the effective size of the sliding window used by the compressor when searching for repetitive strings in the clear text data block. Larger history tables improve the probability of finding repeating strings and can result in higher compression ratios. The use of smaller history tables can provide a moderate decrease in gate area of the LZRW3 core. Many applications, such as disk controllers, have captive compression/decompression architecture and can achieve reasonable compression ratios with 4KB history tables.

Data Flow Description

Data flow through the compressor begins with the detection that the history window is empty. The core requests data from the host until enough look-ahead has been buffered. As data is processed, the distance between the point of processing and previous data fill becomes "the history." The filling process maintains a configurable amount of history. In order to make the history continuous, the history space must be twice the size of the history window and the window halves must be periodically flipped. In parallel with the fill operation the compressor creates records of 3 byte strings through the use of a hashing algorithm. Each byte in the window is processed with the previous two bytes behind it and each new triplet is hashed in order to index a hash table containing the offset into the history where the triplet resides. The output produced contains lengths of matching strings and the hash index, which can be used by the decompressor's hash table to control the copy operation, thereby replicating matching data.

Resource Requirements

CebaTech's LZRW3 IP core targets both ASIC or FPGA applications. CebaTech's unique ESL flow allows timing, area and performance optimizations based on customer's requirements. For information related to your specific application needs, please contact us at sales@cebatech.com.

About CebaTech

Headquartered in Eatontown, NJ, CebaTech, Inc. is a privately held, venture-backed company focused on developing ESL tools and intellectual property modules that accelerate the development and realization of complex software algorithms in silicon. Information about the company and its products may be found at www.cebatech.com

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