CebaTech
The software to silicon company™

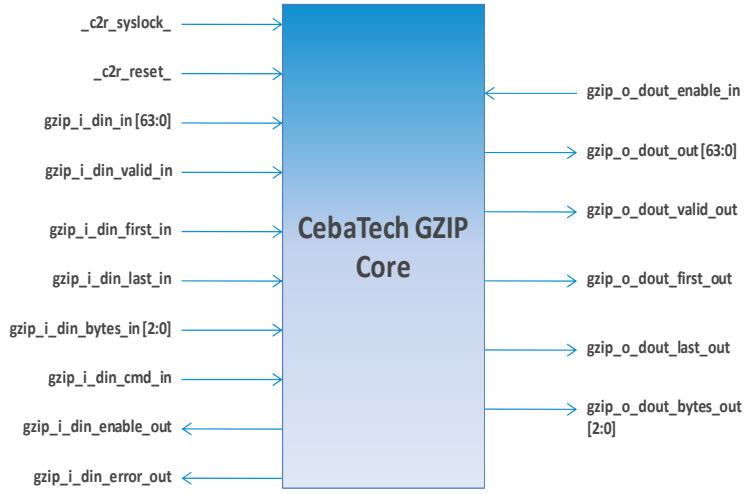
GZIP Data Deflate Core

Overview

CebaTech's family of industry standard GZIP IP cores, based upon the popular software lossless data compression algorithm, provide state of the art hardware compression and decompression to meet demanding data storage and networking needs. CebaTech's hardware implementation of GZIP is in the form of a standalone soft core that performs the deflate function. CebaTech's GZIP core precisely follows the data formats defined by the deflate standard, RFC 1951, and supports frame formats for "GZIP" RFC1952 and "ZLIB" RFC1950.

The GZIP algorithm is implemented using a variation of LZ77 (Lempel-Ziv 1977) and Huffman encoding. GZIP/GUNZIP was written in C by Jean-loup Gailly and Mark Adler and is free of patented algorithms.

The GZIP family of cores enable complete FPGA or ASIC solutions for applications such as real-time WEB servers using HTTP compression, data storage backup systems (disk, tape or even flash based systems), and



Deliverables

- Synthesizable Verilog™ RTL Source
- Verilog test bench with test scripts
- System C Model for rapid prototyping and verification
- Comprehensive User's Guide
- FPGA based evaluation platforms

CebaTech's GZIP Features

- Self-contained, standalone soft core suitable for ASIC and FPGA targets
- Fully synchronous design
- Fully compliant with RFC1951, RFC1952, and RFC1950
- Optional dynamic Huffman tables (max compression)
- Customizable history window sizes (4KB, 8KB, 16KB, 32KB)
- Configurable hash table length to optimize memory area
- Benchmark compression ratios of 2:14 or 3:14 based on Huffman table configuration
- Throughputs from 1Gbps to 64Gbps
- FIFO-based stream interface or optional PCIe core DMA interface

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GZIP Configuration and Performance

Multiple configuration and run-time options for CebaTech's GZIP core provide for tremendous flexibility to match the core characteristics with the user application. Configuration time options determine how the core is built, and impact performance in terms of compression, throughput and area. Run-time options determine how the core is operated, and impact performance in terms of compression ratio and throughput. These features, along with the option to tile the GZIP core to scale throughput, enable CebaTech to rapidly

Configuration Option	Description
Window Size	History Window size, in Kbytes. Valid history window sizes are 4KB, 8KB, 16KB, and 32KB
Hash Bits	With of Hash. Valid hash widths are 12, 14, and 15 bits
Huffman Encoding	Dynamic (DHT) or Static (SHT) Huffman encoding
Fast Clock Rate	Adjusts pipeline stages and clock rate to trade-off area vs. throughput
Default Max Chain	Default maximum hash chain length
Default Good Match	Default maximum for string compares

Run-Time Option	Description
RFC1951	Output DEFLATE encoded blocks only, RFC1951 compliant
RFC1952	Output GZIP encapsulated blocks, RFC1952 compliant
RFC1950	Output ZLIB encapsulated blocks, RFC1950 compliant
Max Chain Length	The maximum depth to which a hash chain is searched
Good Match Size	A match length which, if obtained, will cause searching on a given hash chain to complete

CebaTech's ESL-based development methodology advantage

All of CebaTech's IP cores are developed using the CebaTech C2R™ compiler and development flow. C2R is an innovative system-level design tool than enables CebaTech to develop hardware solutions in ANSI C and compile customer-specific solutions to Verilog RTL.

CebaTech's unique development methodology enables rapid, customer-driven, IP core configurability. IP Core interfaces can be adapted to meet exact customer integration requirements.

IP Core Resource Requirements

CebaTech's GZIP compression and decompression cores are suitable for ASICs and FPGAs. Resource requirements vary greatly based on the configuration required for a specific application.

Using the C2R development methodology, CebaTech works with each customer to develop application specific IP core requirements and helps customers evaluate the various core configuration options to ensure optimum application-level solutions. Contact sales@cebatech.com to start your customized IP core evaluation today!

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