

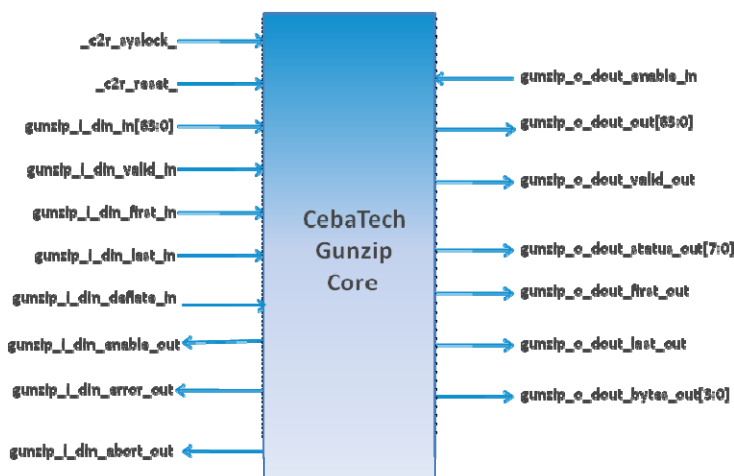
GUNZIP Data Inflate Core

Overview

CebaTech's family of industry standard GZIP IP cores, based upon the popular software lossless data compression algorithm, provide state of the art hardware compression and decompression to meet demanding data storage and networking needs. CebaTech's hardware implementation of GUNZIP is in the form of a standalone soft core that performs the inflate function. CebaTech's GUNZIP core precisely follows the data formats defined by the deflate standard, RFC 1951, and supports frame formats for "GZIP" RFC1952 and "ZLIB" RFC1950.

The GZIP algorithm is implemented using a variation of LZ77 (Lempel-Ziv 1977) and Huffman encoding. GZIP/GUNZIP was written in C by Jean-loup Gailly and Mark Adler and is free of patented algorithms.

The GZIP family of cores enable complete FPGA or ASIC solutions for applications such as real-time WEB servers using HTTP compression, data storage backup systems (disk, tape or even flash based systems), and



Deliverables

- Synthesizable Verilog™ RTL Source
- Verilog test bench with test scripts
- System C Model for rapid prototyping and verification
- Comprehensive User's Guide
- FPGA based evaluation platforms

CebaTech's GUNZIP Features

- Self-contained, standalone soft core suitable for ASIC and FPGA targets
- Fully synchronous design
- Decompresses data previously compressed by any compressor compliant with RFC1951, RFC1952 (GZIP), and RFC1950 (ZLIB)
- Decodes both Static (SHT) and Dynamic (DHT) Huffman tables.
- Customizable history window sizes (4KB, 8KB, 16KB, 32KB)
- Throughputs based on configuration ranging from 1Gbps to 64Gbps
- FIFO-based stream interface or optional PCIe core DMA interface
- Easily combined with CebaTech's GZIP Compression core for a complete solution

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GUNZIP Configuration and Performance

Multiple configuration and run-time options for CebaTech's GUNZIP core provide for tremendous flexibility to match the core characteristics with the user application. Configuration time options determine how the core is built, and impact performance in terms of throughput and area. Run-time options determine how the core is operated, and impact performance in terms of throughput. These features, along with the option to tile the GUNZIP core to scale throughput, enable CebaTech to rapidly deliver a broad range of advanced hardware compression solutions.

Configuration Option	Settings	
Window Size	4KB, 8KB, 16KB, 32KB	<p>History Window size. Defines the size of the sliding window used by the GUNZIP core. The compressed data stream contains pointers to this window which are used by the GUNZIP core during the decompression process.</p> <p>A GZIP compliant decompressor must use a 32KB window size to ensure For captive applications where there is a known "smaller" maximum history window size in the compressor, a corresponding smaller window size can be used in the GUNZIP core to reduce on-chip SRAM requirements. This is common in storage applications.</p>

CebaTech's ESL-based development methodology advantage

All of CebaTech's IP cores are developed using the CebaTech C2R™ compiler and development flow. C2R is an innovative system-level design tool than enables CebaTech to develop hardware solutions in ANSI C and compile customer-specific solutions to Verilog RTL.

CebaTech's unique development methodology enables rapid, customer-driven, IP core configurability. IP Core interfaces can be adapted to meet exact customer integration requirements.

IP Core Resource Requirements

CebaTech's GZIP compression and decompression cores are suitable for ASICs and FPGAs. Resource requirements vary greatly based on the configuration required for a specific application.

Using the C2R development methodology, CebaTech works with each customer to develop application specific IP core requirements and helps customers evaluate the various core configuration options to ensure optimum application-level solutions. Contact sales@cebatech.com to start your customized IP core evaluation today!

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