



Company Backgrounder

CebaTech Inc., develops electronic system level (ESL) tools and high-value intellectual property (IP) cores designed to accelerate the realization of complex software algorithms into silicon and to improve the productivity of engineering teams focused on advanced SoC, ASIC and FPGA systems design. CebaTech's products include IP cores for networking, storage, communication systems and servers, as well as ESL technology for design entry and verification that eliminates development process bottlenecks, reduces costs and accelerates time to market.

COMPANY BACKGROUND

Founded in 2004, the idea that led to the company's inception came from the founders' experiences developing a full gate-level hardware implementation of the TCP/IP protocol stack to create a 1Gbps transport offload engine (TOE). Although successful, that endeavor made it clear that the next step in performance, 10Gbps, for a full stack TOE would require a radically new approach to IC design that could accelerate both the design creation and the functional verification steps of the process. With that as its charter, CebaTech developed the C2R Compiler™, the first system-level design tool to unify design modeling, architecture exploration, verification and implementation in a single design methodology capable of supporting full-chip designs. In addition to the C2R Compiler, CebaTech licenses C2R Compiler-generated IP blocks to hardware developers in high-growth markets, with an initial focus on high-performance IP for the fast evolving storage and networking markets.

CebaTech Inc. is a privately held company located at 444 Route 35 South, Building B in Eatontown, New Jersey. The company's products target engineering teams working on advanced SoC, ASIC and FPGA systems design. These engineers span the semiconductor, networking, computing, storage and mobile technology industries.

THE TEAM

The CebaTech team is made up of experienced business managers, engineers, marketing and sales professionals with deep and wide experience in semiconductor tools development, communication systems, storage design, and manufacturing in large corporations. Together with investors 2M Companies, SAS Investors, and NJTC Venture Fund, the team has the knowledge and expertise required to build and grow a solid and successful company. The executive team includes:

Ramana Jampala, CEO
Chad Spackman, Co-Founder and CTO
Adrian Port, Co-Founder and Chief Technologist
Larry Lipke, VP of Engineering
Elaine Jones, VP of Sales and Marketing

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THE MARKET

While the ecosystem around semiconductor design (shrinking silicon geometries, growing FPGA capacities, and system-on-chip (SoC) techniques) has enabled more and more complex function to be moved into silicon, the design process itself has become an impediment to engineering productivity and to realization of the full application potential of modern integrated circuits (ICs). Reducing the risk of error and re-spins, along with costs, are objectives common to every hardware/chip development team. However, the tools used to accomplish design description, particularly those at the front end of the design process, have not materially advanced in over a decade. Today's complex chips are, for the most part, still developed using the manual, register transfer level (RTL) hardware description language (HDL) established for simpler systems. Verification of the RTL designs is, in turn, a labor-intensive process requiring circuit simulators and customized stimulus, and becomes self-limiting with the increase in design scope or complexity.

Adding resource to design teams is often the answer to complexity challenges – a solution that is neither efficient nor cost-effective. Alternatively, design approaches that incorporate intellectual property (IP) reuse and 3rd party IP design are increasingly used to mitigate risk and accelerate time to market.

CEBATECH PRODUCTS AND APPLICATIONS

CebaTech's is focused on creating products that overcome several obstacles that semiconductor designers encounter in developing high-function silicon. As such, CebaTech's products include both the enabling tools and selected high-value IP blocks for deployment into networking and storage communications solutions. CebaTech's products target engineers of field-programmable gate arrays (FPGA's), Application Specific IC's (ASICs) and System on Chip (SoC) designs.

ESL DESIGN TOOLS

CebaTech's C2R Compiler™ targets the design entry and verification steps of IC design by automating the compilation of ANSI C software into correct Verilog™ RTL for hardware and allowing hardware engineers to adapt software test methods to validate designs.

With untimed ANSI C as the starting point, the C2R Compiler is differentiated in three important ways:

- C2R supports the majority of the abstract and powerful capabilities of ANSI C, with very few exceptions;
- C2R supports small to large design scale and scope, enabling the realization of the most complex designs; and
- C2R places functional verification at the front end of the design process and provides for 95% test coverage in the C software environment.

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Using ANSI C software behavioral modules to make system-level trade-offs and to perform functional tests prior to committing to hardware allows a designer to achieve tremendous improvement in verification time over RTL event-based simulation and enables broader test coverage with available resource.

CebaTech's C2R Compiler supports both control- and data path-dominated designs and works equally well for FPGAs, ASICs or SoCs. By automating the development path from standard ANSI C code to synthesizable RTL, CebaTech dramatically reduces the time it takes to create, explore and implement a hardware design. By providing a direct linkage between the original C design model and the final hardware instantiation and accelerating the verification process CebaTech improves engineering productivity, schedule predictability, and overall quality. As an added benefit, CebaTech's breadth of support for standard ANSI C allows IC design teams to derive hardware from existing, proven software with relative ease.

IP CORES

CebaTech's unique C2R Compiler allows the company to rapidly deliver IP blocks that provide industry-leading function and reliability, as well as to extend the range of IP blocks quickly, and in response to changing customer requirements or network standards. Leveraging its position as an ESL innovator along with its IP design expertise the company engages in joint IP development with end-users, 3rd party design houses and other IP Core vendor partners.

CebaTech also offers its own C2R Compiler- generated IP blocks, the CebaIP™ family of cores, for licensing by hardware developers in the storage and networking markets. Current IP core offerings include:

- GZIP data compression based upon the same software code used for the very popular GZIP software program. CebaTech's GZIP is standards-based and conforms to the popular "deflate" standard as specified in RFC1951. File formats for both ZLIB and GZIP, as specified in RFC1950 and 1952, are also supported. CebaTech offers a single core that operates at approximately 1Gbps rates and that can be "tiled" to operate at higher aggregated stream rates of up to 10Gbps maximum.
- GunZip data decompression, based upon the same software code base for the very popular GZIP software program. CebaTech's GunZip is compatible with both hardware- and software-generated GZIP compressed files. CebaTech offers a single core that operates at approximately 2Gbps rates.

In addition, CebaTech provides turnkey integrated circuit (IC) solutions for select customers that leverage CebaTech's high-value IP along with its tool suite. The resulting FPGAs and/ or ASICs can be an embodiment of CebaTech's IP integrated with a customer's existing design or entirely the customer's original design.